REMARKS

Claims 1, 3-7, 13-18 and 20-22 and new Claim 23 are remaining in the case. Claims 1, 3-7, 13-18, and 20-22 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Karnik (Karnik '527), US patent no. 5,724,527. The Specification has been amended to correct a minor typographical error. In addition, Claims 1, 3, 4, 7, 13, 17, 18, 20, and 21 have been amended and new Claim 23 has been added. Reconsideration of this application is respectfully requested.

Claim Rejections -35 USC § 102(b)

The Examiner has rejected claims 1, 3-7, 13-18 and 20-22 under 35 U.S.C. 102(b) as being unpatentable over Karnik (Karnik '527), US patent no. 5,724,527. However, Karnik '527 fails to disclose, teach or suggest all limitations for each rejected claim. Accordingly, the Office Action has failed to make a prima facie case of anticipation for any claim, and such rejections should be withdrawn.

Karnik '527. The Karnik '527 reference teaches a multiprocessor boot protocol for a multiprocessor system that includes an APIC (advanced interrupt controller) bus as well as a system bus. See Fig. 3 of Karnik, which shows both an APIC bus 20 and an external bus 30. See also Col. 6, lines 36 – 40 "the multiprocessor boot protocol utilized in the computer system of the present invention makes use of an implementation of an advanced processor interrupt controller architecture that defines a multiprocessor interrupt control mechanism."

The Karnik '527 boot algorithm utilizes APIC bus serialization to achieve atomicity – only one message is allowed to exist on the bus at a given time. Karnik, Col. 6, lines 46 – 48. The boot interprocessor interrupt (BIPI) is an APIC message that is sent over the APIC bus. See

Col. 6, lines 51 – 53. Only one processor's BIPI actually executes on the APIC bus. See Col. 6, 56 – 58. The BIPI is a message, not a stall signal.

The Karnik '527 boot algorithm determines a bootstrap processor depending on, in part, which processor completed its initialization and issued the BIPI message first. See col. 6, lines 55 – 62 and Col. 8, lines 9 – 12 ("Determination of the BSP depends on ... which processor happens to issue a BIPI message first").

Claim 1. Claim 1, as amended, recites "determining whether each processor is asserting a stall signal ***on a system bus***." Claim 1, in part. The Office Action fails to make a prima facie case of anticipation of amended Claim 1 because it does not teach the italicized limitation. That is, Karnik '527 teaches a boot protocol that utilizes an APIC bus and does not disclose determining whether each processor is asserting a stall signal *on a system bus*.

Furthermore, the Office Action fails to make a prima facie case of anticipation of amended Claim 1 because the cited reference does not teach determining whether each processor is asserting a *stall signal*.

Karnik '527 teaches away from the limitations of Claim 1. Claim 1, as amended, recites "determining whether ***each processor*** is asserting a stall signal on a system bus." Claim 1, in part. As is mentioned above, Karnik '527 teaches that only one processor at a time can execute a BIPI on the APIC bus. Each processor cannot execute a BIPI on the APIC bus at the same time in the boot scheme disclosed by Karnik '527. Accordingly, Karnik '527 teaches away from the Claim 1 limitations.

Finally, Karnik' 527 also teaches away from the following limitation of Claim 1: "selecting a bootstrap processor from among the operable processors irrespective of an

initialization time of a particular operable processor". As is discussed above, the BSP of Karnik '527 is selected based on which processor first completes its BIST and sends a BIPI message. See Col. 6, lines 54 – 56 and Col. 8, lines 9 – 13.

Accordingly, the Office Action fails to make a prima facie case of anticipation of Claim 1, at least because there is absolutely no disclosure, teaching, nor suggestion in the cited art for "determining whether each processor is asserting a stall signal on a system bus" nor for "selecting a bootstrap processor from among the operable processors irrespective of an initialization time of a particular operable processor."

Claim 1 is allowable for at least these reasons. In addition, Claims 3-7, which depend from Claim 1, are also allowable for at least these reasons.

Claim 13. Regarding Claim 13, the Office Action states that claims 13 – 17 are rejected for the same reason set forth in the Office Action regarding Claim 1 and Claims 3-7. However, the rejection of Claims 1 and 3-7 do not address all elements that appear in Claim 13, as amended. Accordingly, the Office Action does not make out a prima facie case of anticipation regarding Claim 13.

The Office Action has wholly failed to make a prima facie case of anticipation at least with respect to the following elements of claim 13: "an arbitration protocol to determine a bootstrap processor from the plurality of processors irrespective of an initialization time of a particular processor" and "logic to ensure that a) *a stall signal has been de-asserted on the system bus by each processor* and that b) at least one processor is operable prior to allowing the operable processors to enter a bootstrap processor arbitration process." Claim 13, in part (emphasis added).

Karnik fails to teach, suggest or disclose de-assertion of a signal on the system bus by each processor. As is discussed above in connection with Claim 1, the Karnik '527 teaches the use of messages asserted on the APIC bus, not the system bus. See Karnik '527, Col. 5, line 49 – Col. 6, line 16 (discussing "five basic message types specific to the present invention" which are all APIC bus messages). The Office Action thus fails to make a prima facie case of anticipation; Claim 13 is allowable for at least this reason.

As is discussed above in connection with Claim 1, the Karnik '527 reference also does not disclose, teach, nor suggest an arbitration protocol to determine a bootstrap processor irrespective of an initialization time of a particular processor. Instead, Karnik '527 teaches away from such limitation. As is discussed above, Karnik '527 teaches that the bootstrap processor will be decided based, in part, on which processor first completes its initialization process and issues the BIPI message. The Office Action thus fails to make a prima facie case of anticipation; Claim 13 is allowable for at least this reason.

Claim 13 is allowable for at least these reasons. Claims 14-17, which depend from Claim 13, are also allowable for at least these reasons.

Claim 18. Regarding Claim 18, the Office Action bypasses the requirements for a prima facie case of anticipation. Instead of addressing each and every element of Claim 18, the Office Action merely states the following: "Karnik teaches the claim method of steps. Therefore, Karnik teaches the claimed computer readable media to carry out the method of steps." However, such shorthand approach fails because there are elements of Claim 18 that have not been addressed in the Office Action. By failing to address each and every limitation of Claim 18, the Office Action has failed to properly state a prima facie case of anticipation regarding

such claim. The Office Action has wholly failed to make a prima facie case of anticipation at least with respect to the following elements of claim 18: a computer readable media, and instructions embedded on the computer readable media. Because no prima facie case has been made out regarding Claim 18, Claim 18 stands in condition for allowance Claim 18 is allowable for at least this reason. Claims 20-23, which depend from Claim 18, are also allowable for at least this reason.

In addition, the Office Action does not make out a prima facie case of anticipation regarding additional elements of Claim 18 as amended. Specifically, the Office Action has failed to make out a prima facie case of anticipation regarding at least the following element of Claim 18: allowing one or more selected ones of the plurality of processors to enter a bootstrap processor arbitration process responsive to both 1) the signal has been de-asserted on the system bus by each of the plurality of processors..." Claim 18, in part.

As is discussed above in connection with Claims 1 and 13, Karnik fails to teach, suggest or disclose de-assertion of a signal on the system bus by each processor. Karnik '527 teaches the use of messages asserted on the APIC bus, not the system bus. See Karnik '527, Col. 5, line 49 – Col. 6, line 16 (discussing "five basic message types specific to the present invention" which are all APIC bus messages). Karnik '527 also teaches that only one processor at a time may execute a message on the APIC bus. The Office Action thus fails to make a prima facie case of anticipation; Claim 18 is allowable for at least this reason. In addition, Claims 20 – 23, which depend from Claim 18, are also allowable for at least this reason.

For the foregoing reasons, Applicants respectfully submit that the applicable rejections have been overcome and must all be withdrawn. All claims are therefore in condition for allowance. Applicants reserve all rights with respect to the application of the doctrine

equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If the Examiner feels that an interview would help to resolve any remaining issues in the case, the Examiner is invited to contact Shireen Bacon of Intel, at (512) 732-3917.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

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